REMARKS

No new matter has been added. The Applicants again request entry of the amendments as set forth in the Appendices hereto prior to examination of the application on the merits.

Respectfully submitted,

Joseph A. Walkowski
Registration No. 28,765
Attorney for Applicants
TRASKBRITT
P. O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: (801) 532-1922

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JAW/df/dlm

VERSION OF SPECIFICATION WITH MARKINGS TO SHOW CHANGES MADE

Please replace paragraph **[0003]** with the following:

[0003] State of the Art: In semiconductor manufacture, a single semiconductor die or chip including a plurality of integrated circuits on an active surface thereof is typically mounted within a sealed package of a silicon-filled epoxy formed thereabout by a process known as transfer-molding. The package generally protects the die from physical damage and from contaminants, such as moisture or chemicals, found in the surrounding environment. The package also provides a lead system for connecting the electrical devices (integrated circuits)[,] formed on the die[,] to a printed circuit board or other higher-level packaging.

Please replace paragraph **[0005]** with the following:

[0005] In many semiconductor applications, formation of conductive bumps or other external conductive elements on the bond pads of a die is desirable, if not necessary, to connect the die to external conductors. The most common applications where conductive bumps or other elements are used include tape automated bonding (TAB), flip-chip attachment of a die to a carrier substrate, and direct chip attachment (DCA) of a die to a carrier substrate. Conductive bumps may comprise metals or alloys[,] including, without limitation, conventional tin\lead solders, or may comprise conductive or conductor-filled epoxies, all as known in the art. Formation of the conductive bumps used in these applications can be accomplished using a variety of commonly known methods, such as deposition onto bond pads by screening or printing, preform ball or bump placement, or ball bumping using wire bonding equipment to form each individual bump *in situ*.

Please replace paragraph **[0007]** with the following:

[0007] Because of relatively high manufacturing costs associated with state-of-the-art metal deposition equipment dedicated specifically to bumping a die for [flip chip] <u>flip-chip</u> attachment, some semiconductor manufacturers have resorted to the aforementioned ball bumping

using conventional wire bonding tools (capillaries) to form conductive bumps over the bond pads. In the ball bumping process, a capillary of the wire bonding tool carries a conductive wire toward a bond pad on which a bump is to be formed. A ball is formed at an end of the wire by heating and melting the metal wire. The wire bonding tool capillary then presses the ball against the planar bond pad and the portion of the wire extending past the ball is cut, leaving a ball bump on the bond pad.

Please replace paragraph **[0009]** with the following:

[0009] Conventional flip-chip IC devices formed according to the aforementioned fabrication processes exhibit a number of shortcomings. For example, since the active surface of the chip is relatively unprotected, being covered only with a thin passivation layer, damage to the chip can occur during attachment of the chip to the carrier substrate. Likewise, such damage to the chip can occur during handling of the chip[,] or while conducting reliability testing of the same. Moreover, directly bumping the relatively delicate bond pads, even with one or more layers of under-bump metallization thereover to facilitate metallurgical compatibility between the bond pad and the metal bump, may itself cause damage.

Please replace paragraph **[0012]** with the following:

[0012] The present invention includes a method of forming a semiconductor device by forming or providing a semiconductor wafer having an active surface defining a large plurality of individual die locations thereon. As used herein, the term "wafer" includes traditional wafer structures as well as silicon-on-insulator (SOI), silicon-on-glass (SOG) and silicon-on-sapphire (SOS) substrates, among other semiconductor substrates known in the art. The active surface of the semiconductor wafer includes bond pads thereon for making external electrical connections. Either the bond pads are provided with intermediate conductive elements thereon or the input/output connections provided by the bond pads are redistributed into a different pattern or array using traces over the active surface, and the intermediate conductive elements formed at the redistributed input/output locations. A grid of channels or troughs is formed, as by scribing with a

wafer saw or etching, between die locations and of sufficient depth to pass through the active surface to an insulative region to isolate individual, adjacent die active surface regions on the semiconductor wafer. A flowable material used to encapsulate at least the active surface of the entire semiconductor wafer is applied thereto to cover the intermediate conductive elements and is then planarized to expose the intermediate conductive elements. The flowable encapsulant material extends into the channel regions, sealing the exposed, lateral edges of the active surface surrounding each individual die location. The intermediate conductive elements are then provided with external conductive elements projecting transversely from the surface of the encapsulant layer, or an anisotropically-conductive (so-called "Z-axis") film may be placed over the substrate. Alternatively, conductive traces may be formed to extend between the exposed ends of the intermediate conductive elements and one or more edges of each die location to form one or more rows of edge connects suitable for [direct chip attach (DCA)] DCA to a carrier substrate. The semiconductor wafer is cut through its entire depth, as with a wafer saw, along the centers of the channel regions to separate, or "singulate," the individual die locations into flip-chip or DCA dice to be individually connected to a carrier substrate. Alternatively, the entire semiconductor substrate or a group of unsingulated dice may be mated to a carrier substrate and bonded thereto using the external conductive elements. As yet another alternative, the exposed ends of intermediate conductive elements alone may be employed as a land grid array for attachment of a die, substrate segment or entire semiconductor substrate to a bumped carrier substrate, and may optionally be provided with larger conductive pads thereover to facilitate connection to the carrier substrate bumps. As still another alternative, conductive traces can be extended from the bond pads across the active surface and down channel side walls between at least some of the individual die locations prior to encapsulation of the active surface of the semiconductor substrate, the trace ends then being exposed during singulation of the dice to form rows of electrical contacts along edges of the singulated dice, or groups of dice which remain together.

Please replace paragraph **[0020]** with the following:

[0020] FIGS. 7A and 7B, respectively, depict a portion of a semiconductor substrate having two adjacent dice with traces extending over a channel or trough therebetween to provide a DCA configuration upon singulation and a singulated die in a DCA configuration with a carrier substrate; and

Please replace paragraph **[0021]** with the following:

[0021] FIG. 8 depicts a computer system incorporating a microprocessor or a memory device, or both, which incorporates a chip scale package manufactured according to the present invention.

Please replace paragraph **[0022]** with the following:

[0022] A fabrication process of the invention is depicted in FIGS. 1A-1F, which figures include a semiconductor substrate 10 having a plurality of bond pads 12 on an active surface 14 thereof, bearing at least one layer 16 of integrated circuitry 18 thereon. For purposes of simplicity, elements common to FIGS. 1A-1F will hereinafter be numbered identically in subsequent figures illustrating other preferred methods according to the present invention.

Please replace paragraph **[0025]** with the following:

[0025] After the formation of bond pads 12, FIG. 1B depicts how a plurality of channels or troughs 26 is formed on the active surface 14 of semiconductor substrate 10 to define individual die locations on substrate 10. As used herein, the term "individual dice" specifically includes, without limitation, partial wafers bearing more than one die as well as single dice. Channels or troughs 26 extend at a depth sufficient enough to pass entirely through the at least one layer 16 of integrated circuitry 18 upon the active surface 14 of substrate 10 and are cut in a grid pattern comprising a first group of mutually parallel channels or troughs 26 which are arranged perpendicular to a second group of mutually parallel channels or troughs 26. The channels or troughs 26 are located to extend along the so-called "streets" between individual

semiconductor die locations on substrate 10, wherein neither active or passive components of integrated circuitry 18, or interconnect structures for same, are typically located. Various types of methods may be utilized to form channels or troughs 26 having different cross-sectional configurations. For example, a beveled or chamfered channel as shown may be formed using a wafer saw blade or an isotropic etch. A laser drill may be used to form a parallel-sided channel, while an etching process, such as dry or plasma etching or wet solution etching, may be used to form channels with either substantially parallel sides or sloped sides, depending upon the anisotropic or isotropic tendencies of the etch employed. Each one of these types of cutting has advantages and disadvantages over the other types and it will be readily apparent to those skilled in the art which applications would be best used under particular circumstances. For example, where deep channels are preferred or required, wafer saw scribing is preferable as it is rapid and accurate. Where small-dimensioned channels with tolerances that must be tightly controlled are preferred or required, dry or wet etches would be utilized.

Please replace paragraph **[0036]** with the following:

[0036] Intermediate conductive elements 40 may be formed in any variety of suitable shapes and sizes so long as the dimensions of the bumps comply with design constraints of the final semiconductor device assembly. For most applications, intermediate conductive elements 40 will preferably be cylindrical[,] or pillar-shaped. However, as a further alternative and as shown in broken lines in FIG. 3, intermediate conductive elements 40 may comprise traces 40t which are formed on active surface 14 to extend from bond pads 12 to a peripheral edge of a device 34, and at least to separation line 46. Thus, when device 34 is severed from substrate 10, the ends 40e of traces 40t are exposed and may be used to abut and contact a row of connectors at the bottom of a slot of a carrier substrate in a DCA configuration.

Please replace paragraph **[0037]** with the following:

[0037] Rather than singulate each and every semiconductor device 34 as shown in FIGS. 1F and 3, a block of semiconductor devices 34 can remain unsingulated in order to

facilitate unitary attachment of the block to a carrier substrate. In such a manner, for example, a plurality of memory dice may be attached as a group (i.e., partial wafer or other semiconductor substrate) to a carrier substrate to form a multi-chip module. An example of such a configuration is depicted in FIG. 4, wherein carrier substrate 50 is provided. For each semiconductor device 34, external conductive elements 32 are patterned in such a way as to conform to a similar pattern of terminal pads 52 on carrier substrate 50. Carrier substrate 50 may be any type of substrate such as, for example, a printed circuit board made from fiberglass resin (i.e., FR-4, FR-5, etc.) or other carrier substrates used and known to those skilled in the art. Once the semiconductor substrate 10 is positioned such that external conductive elements 32 align with the terminal pads 52 on the surface 54 of carrier substrate 50, the entire assembly may be heated to such a temperature as to cause the external conductive elements (if solder) to reflow and metallurgically attach to the terminal pads 52. With channels or troughs 26 extending through the active surface 14 of substrate 10, each semiconductor device 34 is isolated from one another electrically, but not physically. The physical connection allows a block of devices to be attached to carrier substrate 50 with high precision and in a single step, rather than discretely attaching each semiconductor device 34 using conventional, single-die flip-chip [aligned]aligner/bonder equipment. Additionally, the close mutual proximity of each semiconductor device 34 provides for a greater circuit density on carrier substrate 50 than would otherwise be provided using the singulated semiconductor device approach of prior systems. Overall operational speed of the assembly will improve because of the closer mutual physical proximity of the semiconductor devices 34. As previously alluded to, complete modules can be fabricated, such as, for example, memory modules, where four, six, eight, or other plurality of semiconductor devices 34 can be readily assembled with a carrier substrate 50 in a single step, resulting in a smaller package with increased performance than otherwise possible with singulated semiconductor devices 34.

VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

21. (Amended) The method according to claim 3, comprising:
placing at least one of said plurality of semiconductor elements with said intermediate conductive elements in alignment with conductive bumps protruding from a carrier substrate; and
electrically connecting said intermediate conductive elements and said conductive bumps.

24. (Amended) The method of claim 23, comprising:
placing at least one of said plurality of semiconductor elements with said external conductive elements in alignment with terminal pads of a carrier substrate; and
electrically connecting said external conductive elements and said terminal pads.

26. (Amended) The method of claim 1, further comprising forming conductive traces over said encapsulant material from said exposed portions of said intermediate conductive elements to at least one channel of said pattern of channels, defining a peripheral edge of at least one individual die location of said plurality so as to define a plurality of laterally spaced edge contacts therealong, and severing said semiconductor substrate in alignment with at least some of said channels including said at least one channel into a plurality of semiconductor elements each comprised of said at least one individual die location, wherein said exposed peripheral edges of said at least one layer of integrated circuitry remain covered with said encapsulant material and said plurality of laterally spaced edge contacts are located along a peripheral edge of a semiconductor element of the plurality.

27. (Amended) The method of claim 26, further comprising aligning said plurality of laterally spaced edge contacts with a plurality of edge connectors of a carrier substrate and electrically connecting the plurality of laterally spaced edge contacts with the plurality of edge connectors.